ABSTRACT

Described are programmable logic devices with configuration memory cells that function both as RAM and ROM. A PLD incorporating these memory cells to store configuration data can be mask-programmed with a customer design, rendering the PLD an application-specific integrated circuit (ASIC). The mask programming can be selectively disabled, in which case each configuration memory cell behaves as a static, random-access memory (SRAM) bit. In this mode, a PLD employing these dual-mode memory cells behaves as a reprogrammable PLD, and can therefore be tested using generic test procedures developed for the PLD. The dual-mode memory cells thus eliminate the burdensome task of developing application-specific test procedures for designs ported from a PLD. As an added benefit, in the ROM mode these memory cells are not susceptible to radiation-induced upsets, so for example, PLDs incorporating these memory cells are better suited for aerospace applications than conventional SRAM-based PLDs.